

WHITE PAPER

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New Portal to the Information Superhighway: The Digital Visual Interface (DVI)

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INTRODUCTION

Computers are radically changing the way people work, play and interact. While frequent improvements are made to the performance and functionality of processors, networks, peripherals and software, the video display—a computer's fundamental interface—has undergone almost no change over the past ten years, except for higher frequencies and resolutions. As new chapters in PC development unfold, the major focus for monitor and graphics controller makers will be to update the connection technology between computers and displays.

The world of electronics is changing. Digital is replacing analog in our lives everywhere. Just as audio buffs hear their favorite tracks from digital CDs rather than analog vinyl LPs, home video systems today feature digital video disk (DVD) players rather than VHS tape machines. Even cell phones are going digital. In the digital realm of computers and networks, the analog cathode ray tube (CRT) remains a steadfast holdout. But this too is beginning to change.

The vast majority of computer video monitors today are connected using an analog VGA (Video Graphics Array) interface, an aging technology that represents the minimum standard for a PC display. In fact, today VGA represents an impediment to the adoption of new technologies such as the digital flat panel (DFP) liquid crystal display (LCD), largely because of the added cost for these systems to support the analog interface. Another fundamental is the degradation of image quality that occurs when a digital signal is converted to analog, and then back to digital before driving an analog input LCD display.

The analog VGA interface is ubiquitous today. In fact, nearly 99 percent of all video displays sold in 1998 were based on analog CRT technology. Yet flat panel displays (FPDs) are beginning to make significant inroads on the CRT's dominance because of lower price levels and their growing popularity. These modern, space-saving monitors are even standard items in computer retail stores today. Unfortunately, without a standard in place for a digital interface, today's digital monitors must either employ the antiquated VGA connector or some sort of proprietary digital interface, complete with its own video card.

Efforts to define and standardize a digital interface for video monitors, projectors and display support systems were begun in earnest in 1996. But the process moved rather slowly in ensuing years, causing concern among manufacturers desperate for a standard. Finally, the Digital Display Working Group (DDWG) came together at the Intel Developer Forum in September 1998 with the intent to put the digital display interface standard effort back on the fast track.

With an ambitious goal of clearing through the confusion of digital interface standards efforts to date, the DDWG set out to develop a universally acceptable specification. The group's initial members included computer industry leaders Intel, Compaq, Fujitsu, Hewlett-Packard, IBM, NEC and Silicon Image, with the latter being the developer of TMDS (transition minimized differential signaling), which is the digital signal protocol used by the Digital Visual Interface (DVI) Specification approved by the group in April of 1999.

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“Good In, Good Out: The Key to a Properly Fed Monitor”

Ask customer support people at any reputable display maker, and you're likely to find that most complaints for poor image quality on CRTs can be traced to incompatible graphics controllers on the motherboard or video display card. In today's cost-driven market, marginal signal quality is not all that uncommon. Prevailing abnormalities seen on CRTs include:

- Waveform distortion (shadows, peaks, rings, streaks, and other anomalies);
- Red green blue (RGB) signal voltage levels poorly adjusted or not well matched (poor color performance) and no user adjustment capability; and
- RGB voltages too low or too high (dim or fuzzy monitor).

A poor-quality analog video signal will look even worse when viewed on a FPD because the image must be sampled—that is, converted from an analog to digital—before it can be viewed the digital monitor. While naturally-suited to a CRT, analog RGB signals are wholly unsuitable for driving FPDs, which use digital controllers. Yet, most flat panel display makers today offer analog interfaces to maintain interoperability with existing analog controllers. To accomplish this task, signals are first converted from the CPU's native digital format to analog RGB, where they are then transmitted across the cable. At the other end, the process is reversed—the analog signal is converted to a digital one to drive the LCD display controller.

A digital interface eliminates this problem, placing image control more firmly in the hands of the monitor maker. For a CRT, the digital signal must be converted to analog, but it is received inherently clear of distortion, and further adjustment can be made entirely within the monitor electronics. Ultimately, the net effect of a digital interface to the end user, whether it's an LCD, CRT or LCD projector, is better display performance.

The DVI standard represents a turning point in the history of display technology. Essentially declaring that the days of analog are numbered for display interfaces, the DDWG's effort represents a comprehensive, well-defined, and highly-suitable specification that describes a dual edged deployment strategy. The first supports both analog and digital, while the second phase does away with analog support altogether. Based on existing standards work, the DDWG's DVI specification delivers a digital display interface that will serve an entire industry, and help bring the digital visual experience to the mass market.

This white paper provides a general overview of DVI, including a brief look at developments leading up to the standard, a technical overview of the interface, and a discussion of its potential impact on the industry and end users.

DISPLAY INTERFACE TECHNOLOGY: 1996-1999

Long Live VGA?

Developed in 1987 by IBM, the VGA interface was originally designed to support a resolution of 640 x 480 pixels and 16 colors. Shortly thereafter, VGA was improved, giving rise to Super VGA or SVGA, which supports an 800 x 600 screen resolution, and then XGA, which supports a 1024 x 768 resolution. These modes were eventually standardized by the Video Electronics Standards Association (VESA), the primary standards body for computer display interfaces. Though VGA-based display adapters today support up to 32 bit colors, and resolutions up to 2048 x 1536, the interface is still designed for an analog-only world.

A key problem with VGA is the inconsistency with regard to signal output quality exhibited by display cards and motherboards across the industry. The crux of the trouble lies with the inherent complexities in dealing with analog, juxtaposed with the system maker's desire to make a profit.

Fundamentally, whenever analog video information is transmitted or stored, any inherent signal noise and distortion contributed by the system are additive (i.e., the effects of each are combined to cause a degradation of image quality). Thus, systems that provides higher quality images are likely to be more costly to develop. Another underlying problem with analog is that once the graphic information is corrupted, it's virtually impossible to remove anomalies in the image.

The Path to DVI

One of the earliest widely-used digital display interfaces is LVDS (low-voltage differential signaling), a low speed, and low voltage protocol optimized for the ultra-short cable lengths and stingy power requirements of laptop PC systems. Still a good fit for notebook and handheld PCs, LVDS remains dominant in the portable environment today.

Standardization efforts took a turn for the worse when a split occurred in early LVDS protocol development efforts between chip makers Texas Instruments and National Semiconductor. The two flavors of LVDS being promoted—National's FPD-Link and TI's Flat-Link—carried different signal levels and different formats for transmitting data. Being fully incompatible with one another, the existence of two versions of LVDS could very well have represented the most serious impediment to digital interface standards efforts at the time.

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Digital display interface technology took a decidedly different turn with the introduction of Silicon Image's PanelLink protocol. Named Transition Minimized Differential Signaling (TMDS), the PanelLink protocol was designed to handle larger LCDs as well as serving remote LCDs connected via longer cables. Although TMDS provides the faster data rates required for higher resolutions and expanded color capability, it requires more power and therefore has garnered little support from within the portable computing industry.

In the end, the PanelLink TMDS protocol earned more backing than LVDS. In time, VESA's Plug and Display (P&D) and Digital Flat Panel (DFP) committees both endorsed TMDS as the basis for a standard digital interface for video monitors, projectors, and display controllers on motherboards and video cards. For all intents and purposes, the digital interface standard effort remained stalled at this point, due in large part to the inevitable delays inherent in reaching agreement with a large group.

DDWG Emerges: DVI is Born

Against the backdrop of a FPD market on the verge of taking off and VESA stuck in a holding pattern, an entirely new standards entity was formed from active VESA participants attending the Intel Developer Forum in September 1998. The Digital Display Working Group (DDWG) was created with the sole intent to establish a universally-acceptable, industry standard digital interface that was display-technology independent.

The underpinning of the group's efforts rested on the concept of openness. All interested parties developed the standard with participation and the intellectual property represented by the final specifications is non-proprietary, and available to registered promoters, participants, and adopters royalty-free.

Other essential elements of the effort include basing the protocol on TMDS, while maintaining backward compatibility for P&D- and DFP-capable systems. The group also established boundaries to simplify implementation of the standard, such as eliminating support for non-essential options like USB or FireWire.

Support for legacy VGA connectors was also a crucial ingredient, yet planned phase-out of this support is integrated into the spec via two-stage deployment. DVI-I (analog/digital), the first stage of implementation, provides support for VGA with an adapter, while DVI-V (digital), the second stage, is incompatible with VGA. The specification also provides for dual TMDS links, making DVI capable of handling the increased bandwidth requirements to support display resolutions including UXGA (1600 x 1200), HDTV (1920 x 1080), and QXGA (2048 x 1536).

One of the greatest challenges facing the DDWG was to coordinate their efforts with VESA. For this reason, the DVI specification was designed to leverage previously-published VESA specifications extensively. This also enables manufacturers to fabricate low-cost implementations and facilitates plug and play interoperability.

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For instance, the VESA Extended Display Identification Data (EDID) and Display Data Channel (DDC) specifications are referenced for monitor identification, while the VESA Monitor Timing Specification (DMT) is referenced for monitor timings. In addition, every effort was made to ensure that DVI was interoperable with existing TMDS implementations. VESA DFP- and P&D-compliant devices can interoperate with a DVI compliant connector with a simple adapter.

Wherever possible, the DDWG also attempted to imbue the DVI specification with qualities to enable migration to future technologies such as “selective refresh.” Many in the industry predict that display refresh will be controlled within the monitor. By selectively refreshing only the portion of the screen that changes (while keeping the rest of the display information in memory), an ergonomically-pleasing high refresh rate can more easily be maintained without increasing the required data rate between the graphics controller and the monitor.

Digital Visual Interface (DVI) Technology

The DVI specification defines a digital interface for use between a computing device and a display device. Its simple low-cost connector provides ample performance to allow system developers to add features appropriate to their specific application. The specification enables manufacturers to implement a complete transmission and interconnect solution or any portion thereof. Transmission using alternative media types such as fiber optic cable is also possible.

To address the wide range of requirements within the industry and to ease the process of transitioning to digital, the DDWG has defined two types of implementation. Two connectors with identical mechanical characteristics are specified; one is digital-only (DVI-V) and the other supports digital and analog signaling (DVI-I). Both connectors present system developers with the opportunity to eliminate legacy VGA connectors altogether.

The comprehensive DVI specification defines the entire computer to monitor interface, including a detailed description of the TMDS protocol developed by Silicon Image, configuration of the TMDS links (up to two), plus connector mechanical specifications and signal pin placement. Anticipated bandwidth requirements and pixel formats supported by DVI are also described. The specification also covers issues such as signal quality characteristics for high data rates, power management, and plug and play.

Interoperability among devices that are fully compliant with DVI is provided for via the specification’s plug-and-play configuration and implementation recommendations. In addition, hot plug and monitor feature detection is also supported.

TMDS Overview

DVI is based on an electrical connection that utilizes transition minimized differential signaling (TMDS) to send graphics data to the monitor. The term “transition minimized” refers to a reduction in the number of high-to-low and low-to-high swings on a signal. “Differential” describes the method of transmitting a signal using a pair of complementary signals. These features are important to providing robust, reliable, high-speed data transmission over a wide range of cable lengths and media types.

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Each TMDS link utilizes three data channels and a clock reference. By integrating up to two TMDS links per connector interface, the DVI specification provides ample bandwidth for large-format digital displays. These two TMDS links share the same clock signal so that when both are in use, the bandwidth required to drive the monitor is divided between them evenly. Once the capability of the monitor is detected, the system automatically chooses whether to enable one or two of the TMDS links.

Scalable Bandwidth

With only a single TMDS link operating, the interface is capable of transmitting data at rates up to 1.65 Gbps (165 Mpixels/sec); in dual-link mode, the data transfer capacity reaches 3.30 Gbps. DVI has the ability to handle any current or proposed digital LCD monitor resolution with room to spare, from 640 x 480 VGA all the way up to HDTV and QXGA at 1920 x 1080 and 2048 x 1536 resolutions respectively.

The amount of bandwidth required for a specific display is technology dependent. For example, CRTs typically specify blanking intervals and time slots when display data must be transferred. This blanking period effectively increases the bandwidth required for the interface. It is anticipated that advances in display technology will reduce and eventually eliminate the blanking overhead requirement, maximizing the amount of bandwidth available over the interface to the display.

A single DVI TMDS link provides enough bandwidth to support resolutions greater than HDTV with the blanking interval reduced. In dual-link mode, DVI can provide the higher bandwidth demanded by displays that do not support reduced blanking, such as high-resolution digital CRTs.

The key difference between a digital CRTs and a conventional analog CRT is that the signals received by the display are digital instead of analog, and digital-to-analog conversion must be carried out within the monitor. While the image quality is likely to be better, digital CRTs will require additional bandwidth overhead for horizontal and vertical retrace intervals. This is facilitated through the use of two TMDS links. For instance, digital CRTs compliant with VESA's Generalized Timing Formula (GTF) at resolutions exceeding 2.75 million pixels at an 85Hz refresh rate are easily supported.

Alternate Media

Since TMDS provides DC balancing, the signaling protocol is adaptable to fiber optic cable. While not covered specifically in the DVI specification, fiber optic implementations are considered to be DVI compliant as long as the specification's plug and play capabilities, such as reading EDID data or hot plug detection, are supported.

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TMDS Link Architecture

The TMDS link architecture consists of a TMDS transmitter that encodes and serially transmits a data stream over the TMDS link to a TMDS receiver. The TMDS specification defines the encoding and decoding requirements for the transmitter and receiver. While the 24-bits wide input data stream will represent a typical implementation, it is not a requirement. The DVI specification does not place a limit on the interface format to the TMDS transmitter or receiver components.

The input streams contain pixel data, control data, a data enable signal, and the clock reference. Depending on the state of the data enable signal, the transmitter encodes pixel data or control data, ignoring one when the other is being transmitted.

The transmitter utilizes three identical encoders per TMDS link, one for each data channel. During the transmit operation, each encoder produces a single 10-bit TMDS-encoded character from either two bits of control data or eight bits of pixel data (depending on the state of DE), to provide a continuous stream of serialized TMDS characters. The clock signal provides a TMDS character-rate reference that allows the receiver to produce a bit-rate-sampling clock for the incoming serial data streams.

At the downstream end, the TMDS receiver synchronizes itself to character boundaries in each of the serial data streams, and then TMDS characters are recovered and decoded. All synchronization queues for the receiver are contained within the TMDS data stream.

TMDS Encoding

TMDS encoding is carried out in two stages. The first stage produces a transition-minimized nine-bit code word made up of an eight-bit representation of the original input, plus a one-bit flag that indicates which of two predefined methods was used to convert the original eight-bit word.

The second stage of the encoder manages the overall DC balance of the transmitted data stream, which produces the TMDS 10-bit code word or character. This is accomplished by selectively inverting the eight data bits of the nine-bit code words produced by the first stage. A tenth bit is added to the code word to indicate when the inversion is performed.

Why Encode?

The coding algorithm defined for TMDS signaling reduces the number of transitions in the data stream, which minimizes electromagnetic interference in copper cabling. Encoding also provides a DC-balanced signal that is required for transmission over alternative media such as fiber optic cables. Another feature of the coding algorithm is that it provides for robust clock recovery at the receiver, enabling high-skew tolerance in applications that employ either very long or low cost cabling implementations.

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Electrical Overview

The TMDS protocol is based on the use of differential signal pairs which provides for long cable lengths and reliable transmission of data. A current source is used at the transmitter to drive a low voltage differential signal at the receiver side of a DC-coupled transmission line. A link reference voltage is used to define the highest DC level of the differential signal, while the lower DC level is fixed by the transmitter current source and the termination resistance at the receiver. Termination resistance and characteristic impedance of the cable must be matched.

Signal integrity requirements for the TMDS link are based on measurements taken at test points TP2 and TP3. Signal tests are not required at points TP1 (the pins of the TMDS transmitter) or TP4 (the pins of the receiver). This approach includes the effects of the network and the transmitter and receiver components, while reducing measurement requirements to only two test points. Cable requirements are simply specified as a maximum signal degradation between points TP2 and TP3.

DVI electrical specifications include system ratings and operating conditions, transmitter- and receiver-specific parameters, cable assembly specifications, jitter provisions, and recommended measurement procedures.

DVI Connection System

A DVI-compliant host system can provide either a digital-only or combined analog-digital interface, and the host connector determines the system's capabilities. The connection receptacle on the system side has two choices for implementation. One is designated DVI-V and supports the digital portion of the interface only. The other, dubbed DVI-I, supports both digital and analog signaling and includes additional pins for the analog interface. Both have identical mechanical characteristics.

For DVI's two defined connectors, the digital signals are always present and the same physical outer dimensions are the same. That way monitors equipped with a digital interface can attach to either DVI system connector. Since the digital-only system connector does not have analog pin sockets, the plug of a DVI-compliant analog monitor cannot be attached.

The digital-analog DVI-I connector is designed for applications with minimal port space or those with special performance requirements. DVI-I includes an analog interface that enables end users to use a DVI connector on the monitor side regardless of whether the display technology is LCD or CRT, or has an analog or digital interface. DVI-I does require an adapter dongle to work with VGA. While digital-only DVI-V can coexist side-by-side with standard VGA to support legacy display systems, both types of DVI connector offer system developers an opportunity to eliminate the legacy VGA connector altogether.

Target applications for DVI-I include conventional desktop PCs that may want to utilize legacy VGA displays. On the other hand, the "digital only" DVI-V connector will not drive an analog VGA display without a D/A converter. Therefore, target uses for DVI-V are digital input displays.

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The mechanical connector for the DVI interface includes definitions for 29 physical signal connections in the DVI-I configuration. These are divided into two sections. The first section is made up of three rows of eight contacts comprising 18 TMDS signaling pins plus shielding, and five pins dedicated for plug and play interoperability. The second section includes six pins designed specifically for analog support (red, green, blue, horizontal and vertical synch, and ground).

Future Enhancements

Scalability

Higher resolution monitors are much easier to implement with digital technology than analog. Digital device performance is directly tied to the state of the art in integrated circuit technology. On the other hand, improvements in digital-to-analog, and analog-to-digital conversion devices are much more difficult to implement, typically requiring new technology at great expense. Digital interface technology such as DVI is the fastest and most efficient path to higher display resolutions in the future.

High Color Depth Support

A future improvement for DVI is likely to come in the form of higher color depth support beyond 24-bits per pixel. This enhancement will be supported via the second TMDS link. The system will be required to identify high color depth capability in the monitor before the feature can be enabled.

Power Management

Digital Monitors

Digital monitor power management is supported via defined power states within the DVI specification. These power states enable the power consumption of the monitor to be incrementally controlled, and are summarized below. Only two of these power states are required for DVI compliance: 1) Monitor On Power State, and 2) Active-Off Power State.

- **Monitor On Power State** — In this state, the TMDS link is active, meaning the transmitter and receiver are both on and active. EDID data is available.
- **Immediate Power State** — The TMDS link is not active and the transmitter is powered down. The receiver remains on so that it can detect the activation of the link. The amount of time that this state is maintained is controlled by a timer and EDID data is available.
- **Active-Off Power State** — The TMDS link is inactive, the transmitter is off, and the receiver is on. EDID data is available.
- **Non-Link Recoverable Off Power State** — The TMDS link is inactive, and both the transmitter and receiver are off. Availability of EDID data is not guaranteed. This state can be exited if the

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DDC +5 volt signal is reactivated at the system interface or the power switch to the monitor is toggled.

- **Monitor Power Switch Off Power State** — This state exists when the power switch to the monitor is turned off. Availability of EDID data is only guaranteed if the DDC +5 volt signal is present at the system interface.

Analog Monitors

DVI compliant devices that employ the analog section of the specification must conform to VESA's Video Signal Standard (VSI) specification, as well as VESA's Industry Standards and Guidelines for Computer Display Monitor Timings specification or the VESA Generalized Timing Formula Standard. In addition, both the host system and the analog monitor must support separate horizontal and vertical synchronization. DVI analog power management compliance is referenced in the VESA DPMS Specification.

Inter-Standard Support

VESA P&D and DFP

Since both the VESA Plug and Display (P&D) and Digital Flat Panel (DFP) specifications are TMDS-based, they include the same signaling protocol and electrical interface as DVI. Interoperability is simply a matter of providing the proper connector adapter. In fact, currently shipping TMDS-based products are DVI compatible today.

VESA Display Identification, Plug-n-Play, and Hot Plug Support

Manufacturers of DVI-compliant systems and monitors are required support some of the more user-friendly VESA standards like plug and play, display capabilities sensing, and hot plugging. DVI compliant devices are currently required to support display capabilities sensing via the VESA External Display Identification (EDID) data structure. EDID 1.2 and 2.0 compliance are recommended today, and support for EDID 1.3 is likely within 12 months of VESA adoption.

To facilitate the implementation of automated sensing and startup capabilities, all DVI-compliant monitors are required to support an industry standard low pixel format (i.e., 640 x 480 pixels, 60 Hz refresh rate, pixel clock of 25.175 MHz, and a horizontal frequency of 31.5 kHz). During system startup, the host BIOS and operating system automatically accesses a display's EDID data structure for information regarding monitor type and capabilities, including pixel formats and interfaces supported. While in low pixel format, the user provides simple inputs based on available pixel formats supported by the monitor and the graphics subsystem, to determine the display format.

Further, EDID compatibility requires that the host and monitor be able to select one or two TMDS links based solely on pixel formats and supported refresh rates. To accomplish this, the primary TMDS link is required to support all pixel formats and timings up to and including a pixel clock rate of 165MHz. If the display's capabilities exceed this limit, two TMDS links are automatically established, with each one configured at exactly half the frequency of the maximum pixel clock rate capability of the display.

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When a digital monitor is detected at system startup, only the primary TMDS link is activated. The secondary TMDS link is only turned on if the graphics controller senses that the monitor can support the second link. If a DVI-compliant analog monitor is identified, the monitor is driven in the same manner as if it were connected to a 15-pin legacy VGA connector.

Hot Plug Detection is incorporated into the specification to allow host systems to determine when a DVI compliant monitor is plugged in after computer boot up. Once a “Hot Plug-In” event is detected, the system automatically queries the monitor and activates TMDS signaling, if required. Hot Plug support is a subset of VESA Plug and Play compliance, and is required for devices to be DVI compatible.

WHY DVI?

DVI technology is truly an enabling technology. It provides benefits to end users and display product manufacturers alike. End users may enjoy lower cost devices, simpler set-up and operation, and an enhanced visual experience for both analog and digital displays.

End-User Benefits

The digital interface has several inherent benefits over the standard VGA connector. For starters, with a FPD a digital interface ensures that all content is transferred in a digital format from creation to consumption, meaning that data integrity is maintained during transmission from host to monitor at the highest possible level. By using a digital interface rather than analog VGA, in general, the average end user will see an improvement, with overall sharper, crisper images quality—regardless whether the display technology employed is CRT or FPD.

Another key benefit of a DVI-based display is that it improves the user’s overall visual computing experience. DVI enables manufacturers to add a whole host of low-cost features and advanced capabilities. Also, digitally-driven CRTs and FPDs require fewer adjustments, resulting in easier operation—an integral component to the Intel/Microsoft-led Easy PC initiative. In fact, one of the biggest benefits of DVI is that it has the capability to significantly minimize the occurrence of end-user problems related to things like set up and image quality. Another side-effect of DVI is that some of the host system’s processing requirements are offloaded, enhancing overall PC performance.

Lower power is another upside for DVI. As more users migrate to FPDs, a likely byproduct of DVI, the power savings to businesses could be significant.

Manufacturer Benefits

The DVI specification also comes at a critical juncture for the FPD industry—precisely at a point when the market is starting to really heat up. The DVI interface has the potential to lower prices for finished products since it simplifies the overall interface, which can lower the cost of components, system development, manufacturing, and test. The DVI specification is destined to promote growth in the FPD industry. It also increases the system developers control over real-world interoperability, which should serve to minimize product returns and technical support costs.

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Conclusions

The DVI standard appears at a crucial stage in the emerging digital FPD market. DVI has the power to lower costs for both end users and manufacturers. At an even higher level, DVI brings continuity to an industry facing an impending proliferation of potentially confusing and incompatible interfaces.

Despite DVI's obvious application for digital displays, it represents a death knell for analog VGA interfaces as well. Incorporating DVI with a traditional analog CRT monitor enables manufacturers to gain added control over final image quality, making differentiation based on image quality much more of a factor than it is today.

THE VIEWSONIC VISION

ViewSonic is committed to the DVI standard, and enthusiastically supports the Intel-led DDWG in its efforts to promote and implement DVI. ViewSonic is the first company to introduce digital CRT displays based on the DVI specification, and the company's OptiSync™ technology will allow users to optimize their display image using either analog, digital, or standard video inputs, and eventually help digital CRTs reach price parity with analog CRTs. ViewSonic is and will continue to do its part in helping to usher in this new era in digital display technology based on the DVI specification.

ViewSonic's commitment to the DDWG and the DVI specification is integral to the company's vision of the role of the FPD as an enabling technology. FPDs provide a glimpse of computing's future, and DVI will enable growth in this promising industry. In fact, display technology may soon become more important than the computer—a paradigm shift we may just be starting to experience today.

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GLOSSARY

Blanking Period

Time on the TMDS link when the data enable signal is inactive and control signal data is present on the link. In contrast, **Active Data Period** is the time on the TMDS link when the data enable signal is active and pixel data is present on the link.

Channel

A TMDS channel is defined as a single differential signal pair.

Control Signals

Non-pixel data that is transmitted over the TMDS link.

Data Enable

A link-control signal that indicates whether pixel data or control signals are transmitted over the TMDS link.

Dual TMDS Link

Six TMDS data channels plus one TMDS clock channel.

Pixel Data

This is the 24-bit red green blue data that is transported over the three data channels of the TMDS link.

TMDS

Transition minimized differential signaling.

TMDS Characters

Encoded 10-bit words that are serialized and transported over the TMDS data channels.

TMDS Clock Channel

A frequency reference signal used to synchronize the TMDS encoded characters received over the TMDS data channels.

TMDS Data Channel

A single serial stream of TMDS encoded data.

TMDS Link

Three TMDS data channels plus one TMDS clock channel.

VESA

Video Electronics Standards Association

